AI-Driven Chip Testing on the Cloud

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Abstract
The semiconductor testing process is a key bottleneck in the chip manufacturing flow. To address this inefficiency, data engineering pipelines have been built in the cloud that unify the ingest of test vectors and rich parametric telemetry for real-time testing and AI-powered diagnosis. New chips are tested using algorithms that can decide whether to release or scrap a chip based on the test results and preceding telemetry. Because clearance decisions are made during test, failed chips can quickly be relabeled or logged without being held in test. Data science pipelines examine failed chips and use the conclusions from these analysis to detect issues in other chips in near real-time. Such AI-powered diagnostics also have the potential to help prevent future recurrences. Acting on these insights can ultimately improve yield and shorten test time for future designs.

Data pipelines are about two orders of magnitude less expensive than the test process. They enable continuous decision-making for testing, clearance, and failure analysis without manual steps and facilitate timely action based on telemetry and failed part diagnostics. Making the testing process more efficient can represent significant cost savings for high-volume products. Ultimately, delivering better and cheaper parts to customers faster improves competitiveness and profitability.

Keywords: Semiconductor testing, semiconductor diagnostics, data engineering, cloudscale development, cloud-scale data engineering .

1. Introduction

Semiconductor generation and testing remain costly and time-consuming processes that benefit from cloud-scale data engineering. High-fidelity semiconductor test vectors are computed in a cloud environment and the test operations of chips are distributed to multiple test systems. The semiconductor testing becomes a cloud-scale data generation system, with the ATE data ingested in real time into cloud-based storage and serving systems. In parallel, an AI-based visual diagnostics pipeline is enabled. High-quality visual diagnosis labels are created to train AI-based visual diagnostics models, thereby providing a scalable solution. High-speed cloud ingestion and storage systems handle the large amounts of diagnostic data generated by the physical testing operations. Real-time AI-based visual diagnosis of the chips and non-intrusive test vector noise analysis enable root-cause analysis on the tested chips. The presented cloud-scale data engineering approach and test-vector-management system enable high-fidelity and real-time semiconductor data generation for AI-powered diagnostics. The AI-powered visual-chip-diagnostic system and the cloud-scale semiconductor ATE ingestion are capable of visual analysis and scaling with only automatic test equipment data.

The successful deployment and operation of high-speed data pipelines focused on the real-time generation of high-fidelity cloud-based data for AI applications are showcased. The methodology enabled is relevant to all data-science and AI disciplines for which high-quality, wide-area data-labeling pipelines and infrastructure are critical. Deep learning is an advanced data-mining technology that continuously pushes the limits of SI systems. At the same time, rubber-stamp manufacturing processes, decreases in the size of semiconductor technologies and constant pressure to find faults at each level, increase the yield and reduce the cost of production are forcing data generation at as high speed as the manufacturing process permits. The ultimate prize is finding a solution to the problem of previous black-box development methodologies of artificial intelligence based chips.

Table 1. Overview of the Proposed Semiconductor Testing Framework

Component	Description	Purpose	Technologies/Approaches
Cloud-Scale Data Engineering	Distributed cloud infrastructure for semiconductor testing data	Real-time ingestion, storage, and analytics	Open-source cloud technologies, streaming systems
Semiconductor Test Systems	Automated Test Equipment (ATE) executing test vectors	Validate chip functionality and quality	Real-time chip testing
Data Lake	Centralized storage repository	Store telemetry, diagnostics, and test measurements	Streaming ingestion, scalable storage
AI-Powered Diagnostics	Machine learning models for failure analysis	Detect defects and improve yield	CNNs, deep learning, predictive diagnostics
Test Vector Management	Organizes and distributes test vectors	Improve test coverage and reduce redundancy	CCTV and TVD strategies
Streaming Serving Layer	Real-time data dissemination layer	Continuous monitoring and diagnostics	Cloud streaming architecture

2. Background and Motivation

With a more connected world, there is a growing need for more interconnected devices, appliances, and systems, and semiconductors are the fundamental building blocks of these

ISSN: 3067-4190
JOURNAL OF ARTIFICIAL INTELLIGENCE AND BIG DATA DISCIPLINES
Volume: 04 Issue: 01
RECEIVED: JANUARY 18 REVISED: FEBRUARY 02 ACCEPTED: FEBRUARY 20 PUBLISHED: MARCH 04

devices, which has attracted investments of hundreds of billion dollars in research facilities and product manufacturing. After an overall picture of this booming market, this section presents the two focal areas of this work with a more academic perspective: semiconductor testing for validating and certifying products, and Artificial Intelligence, drawing bridges between those two areas. Real-time data engineering processes, transported from the cloud to the edge, seize test signals and guarantee a method to generate the best test samples for advanced kayseq technologies.

An increasing number of products and systems are based on Artificial Intelligence techniques, such as information classification, image processing, anomaly detection, speech recognition, information generation, and many others. Nevertheless, many products are restricted to specific applications, and the potential empowered by these Artificial Intelligence techniques will only be accessible for all products when the development of high-quality information labeling tools and processes finally breaks the existing barriers. One of those barriers is the lack of high-quality labeled information, especially for training models that classify information in abnormal behavior and during testing for edge inference. One of the AI models in this work aims to help build high-quality labeled information repositories for semi-conductors, boosting test coverage for these products that necessarily play a central role in enabling the integration of AI techniques in all products and systems.

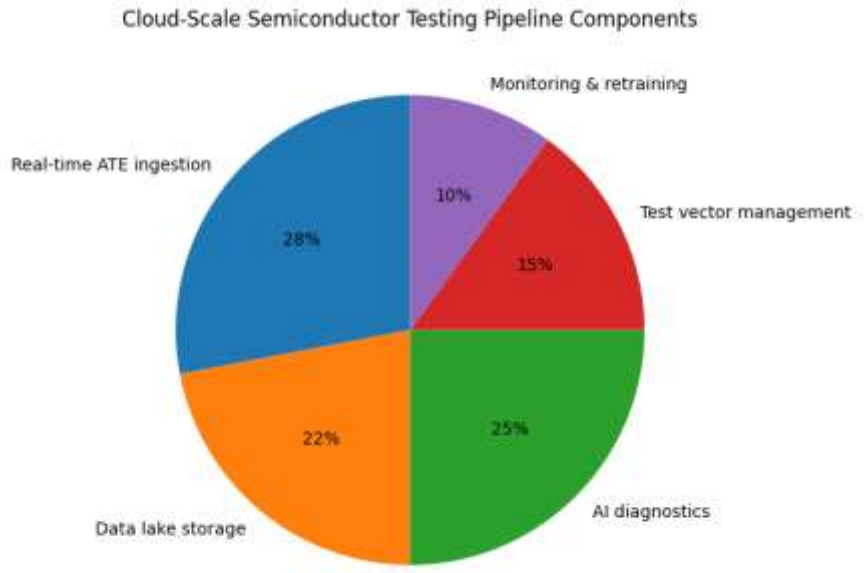

Table 2. Real-Time Data Engineering Pipeline

ISSN: 3067-4190
JOURNAL OF ARTIFICIAL INTELLIGENCE AND BIG DATA DISCIPLINES
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Pipeline Stage	Input Data	Processing Activity	Output
Data Generation	Semiconductor test vectors and telemetry	Functional testing of chips	Raw test data
Data Ingestion	ATE measurement data	Continuous upload to cloud	Streamed semiconductor data
Data Storage	Streaming data	Storage in cloud data lake	Structured datasets
AI Diagnostics	Historical and live test data	Predictive analysis and classification	Failure diagnostics
Monitoring & Analytics	Diagnostic outputs	Visualization and root-cause analysis	Yield optimization insights
Feedback Loop	AI-generated insights	Test vector improvement	Enhanced future testing

3. System Architecture for Cloud-Scale Data Engineering

A distributed architecture based on open-source cloud-scale data engineering principles establishes a cloud-scale solution stack that ingests, processes, and distributes semiconductor test data in real time. Cloud-scale computing enables data engineering systems that perform the requisite data processing and data movement at something approaching the required rates for industrial applications. Relatively small volumes of data are created and made available within seconds to hopefully help engineers narrow the root cause analysis as fast as possible. For semiconductor devices previously subjected to real-time diagnostic tests, the data is used to power a suite of AI-based diagnostics running in urban legend.

The first component of the architecture is a streaming serving layer designed to facilitate the dissemination of the data up and down the testing process from various levels of testing (wafer, package, board, system) to the diagnostic model developers and back. This layer is complemented by a test vector management system that organizes and processes the test vectors delivered to the tester during production testing. Together with the previous component, they provide the requisite data flow for real-time monitoring of semiconductor testing.

Mathematical Formulas:

1. Signal-to-Noise-and-Distortion Ratio (SINAD)

Used in semiconductor diagnostics and test-quality evaluation.

$$SINAD = 10\log_{10}\left(\frac{P_{signal} + P_{noise} + P_{distortion}}{P_{noise} + P_{distortion}}\right)$$

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2. Data Throughput Equation

Represents streaming data ingestion performance in cloud pipelines.

$$Throughput = \frac{Data\ Volume}{Processing\ Time}$$

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3. Chip Yield Formula

Useful for semiconductor manufacturing efficiency.

$$Yield = \frac{Number\ of\ Good\ Chips}{Total\ Chips\ Tested}$$

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4. Classification Accuracy

Applied in AI-powered chip diagnostics.

$$Accuracy = \frac{TP + TN}{TP + TN + FP + FN}$$

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5. Precision of Failure Detection

Measures diagnostic correctness.

$$Precision = \frac{TP}{TP + FP}$$

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6. Recall for Fault Detection

Useful in semiconductor anomaly detection.

$$Recall = \frac{TP}{TP + FN}$$

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7. Latency in Real-Time Streaming

$$Latency = Processing\ Time - Arrival\ Time$$

8. CNN Convolution Operation

Related to AI-based chip image diagnostics.

$$F(i,j) = \sum_{m} \sum_{n} I(i-m, j-n) K(m,n)$$

9. Mean Squared Error (MSE)

Used during AI model training.

$$MSE = \frac{1}{n} \sum_{i=1}^{n} (y_i - \hat{y}_i)^2$$

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10. Data Compression Ratio

Useful for cloud-scale storage optimization.

$$Compression\ Ratio = \frac{Original\ Size}{Compressed\ Size}$$

11. Failure Probability

$$P(Failure) = \frac{Failed\ Chips}{Total\ Chips}$$

12. Test Coverage Equation

$$Coverage = \frac{Detected\ Faults}{Total\ Faults}$$

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13. AI Model Loss Function

Binary classification for pass/fail chip prediction.

$$Loss = -[y\log(\hat{y}) + (1-y)\log(1-\hat{y})]$$

14. Streaming Queue Utilization

$$Utilization = \frac{Arrival\ Rate}{Service\ Rate}$$

15. Cloud Storage Scaling

$$Storage_{total} = N \times Storage_{per\ chip}$$

3.1.DataIngestionandStreaming

The first layer of the cloud-scale data architecture addresses the use case of real-time semiconductor testing. A key requirement is the ingestion of measurement data that is generated during semiconductor tests at a 24-by-7 scale. Each test of a semiconductor device requires the execution of test vectors that are applied to the device terminals, and the test results are returned to the testing system and stored in a SQL storage system. An

ISSN: 3067-4190
JOURNAL OF ARTIFICIAL INTELLIGENCE AND BIG DATA DISCIPLINES
Volume: 04 Issue: 01
RECEIVED: JANUARY 18 REVISED: FEBRUARY 02 ACCEPTED: FEBRUARY 20 PUBLISHED: MARCH 04

efficient data upload system is provided to continuously gather test measurement data from these SQL systems at the end of every test into streaming storage of a data lake.

The data-lake serving these test measurements also supports the use case for AI-generated chip test diagnostic data and leverages the streaming ingestion of chip test measurement data from the real-time chip test system.

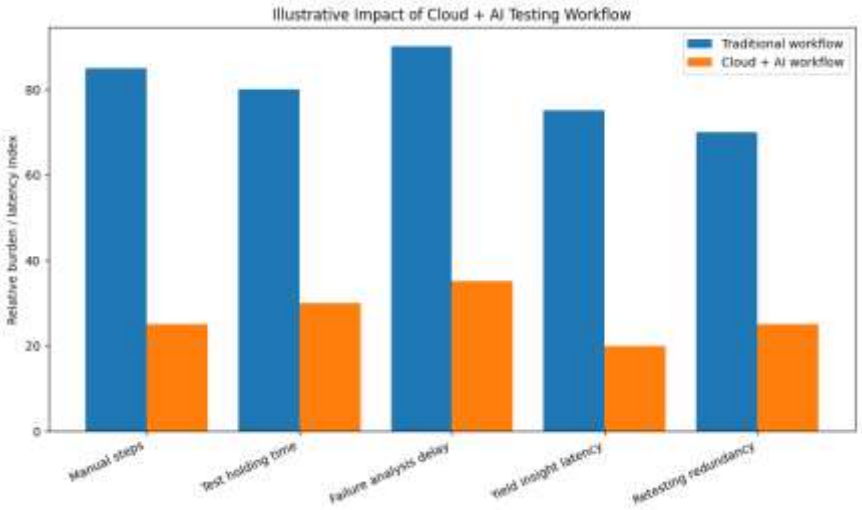

Table 3. Semiconductor Testing Workflow

Stage	Activity	Objective	Result
Test Vector Generation	Create functional test patterns	Stimulate chip functions	Test matrix
Functional Testing	Execute vectors on semiconductor devices	Validate chip behavior	Response measurements
Signal Analysis	Compare outputs with expected values	Detect deviations	SINAD assessment
Data Logging	Store simulation and test logs	Trace chip behavior	Diagnostic datasets
Failure Analysis	Analyze abnormal responses	Identify root causes	Failure classification
AI-Based Recommendations	Predict corrective actions	Improve production quality	Yield enhancement

4. Real-Time Testing Pipelines for Semiconductors

The core of semiconductor testing consists in the assessment of chip responsiveness to thousands of functional patterns, called test vectors. Test vectors characterize the chip functions of interest and are explicitly defined by the chip designer. To disseminate these vectors, a dedicated Test Pattern Generator (TPG) is implemented. The test matrix produced by the TPG serves as input for various semiconductor testers or channels. Each test vector stimulus activates the chip, and the chip response is measured and compared to the expected output.

In parallel, an industry-standard register transfer-level simulation set-up provides logging coverage of all stimulated chip functions, offering a baseline to determine the quality of chip test results as well as the reasons for any eventual failure. The test matrix from the TPG, combined with the simulation log coverage and the results from all testing channels, enables the generation of a Signal-to-Noise-and-Distortion Ratio (SINAD) assessment for the chip functions, which is essential for diagnosis.

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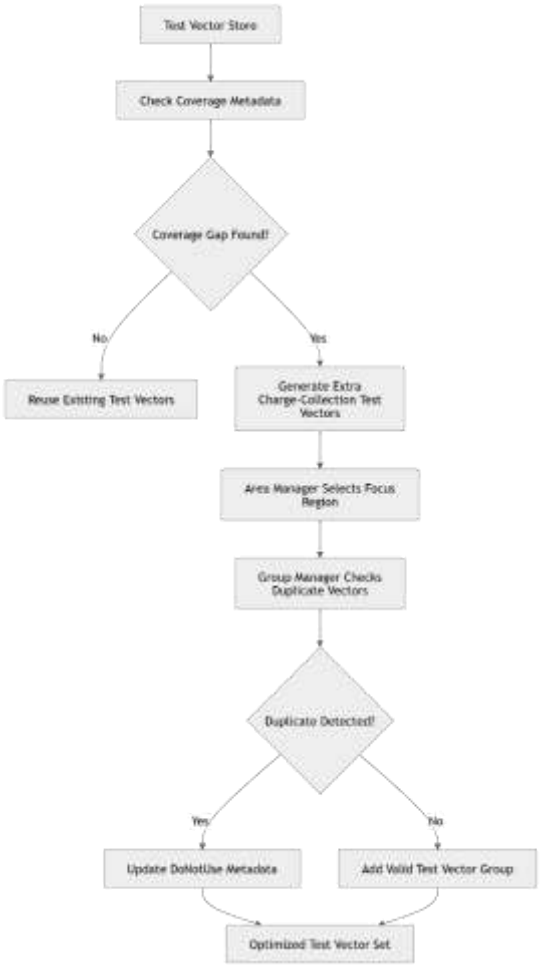

4.1.TestVectorManagement

Test vectors are the input patterns used to stimulate a silicon chip when testing it after fabrication and are cached and reused in final test. Charge-Collection Test Vectors (CCTV) are specifically for detecting charge-collection defects caused by radioactive particles. They check if charge injected into the chip is trapped in the oxide near the MOSFET channel and can leak through the oxide. These defects tend to only trigger a handful of test vectors, so a careful selection and categorization process is needed for future tests. Other test vectors are for detecting gaps in the testing space. Typically, for CTVs, if a small part of the chip has already been tested with a CCTV, the DoNotUse metadata is updated to prevent redundancy.

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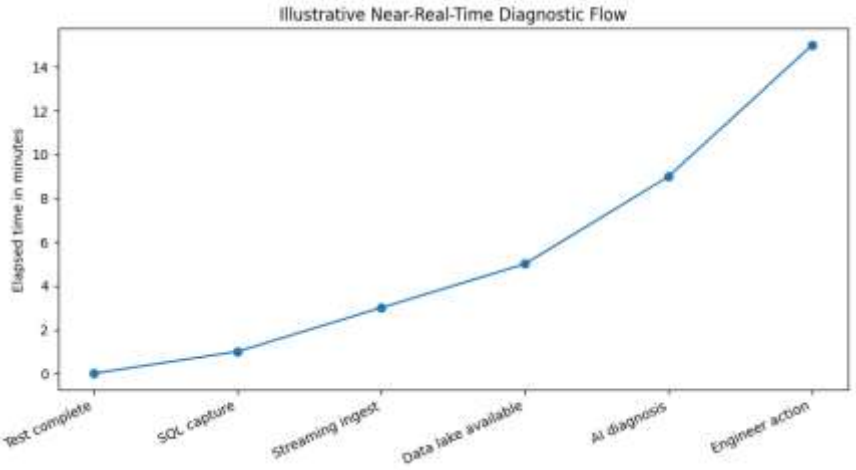

The extra TVD management uses groups of CTVs and is triggered when the TX store is populated enough. Four stages help decide whether to generate extra CTVs, determine which area to focus on, how many areas to cover, and the distribution of the test vectors based on missing coverage. This management is adapted for the extra TVD generator. When a duplicate is detected, the group manager update the valid DoNotUse area and moves to the group with the same area received from the area manager.

Table 4. Test Vector Management Strategies

Strategy	Description	Benefit
Charge-Collection Test Vectors (CCTV)	Detect charge-collection defects caused by radioactive particles	Improve defect identification
DoNotUse Metadata	Prevent repeated testing in already-covered areas	Reduce redundancy
Extra TVD Generation	Generate additional vectors for uncovered regions	Improve test coverage
Group-Based Vector Management	Organize vectors into coverage groups	Efficient vector allocation
Duplicate Detection Mechanism	Detect overlapping vector coverage	Optimize resource utilization

5. AI-Powered Chip Diagnostics

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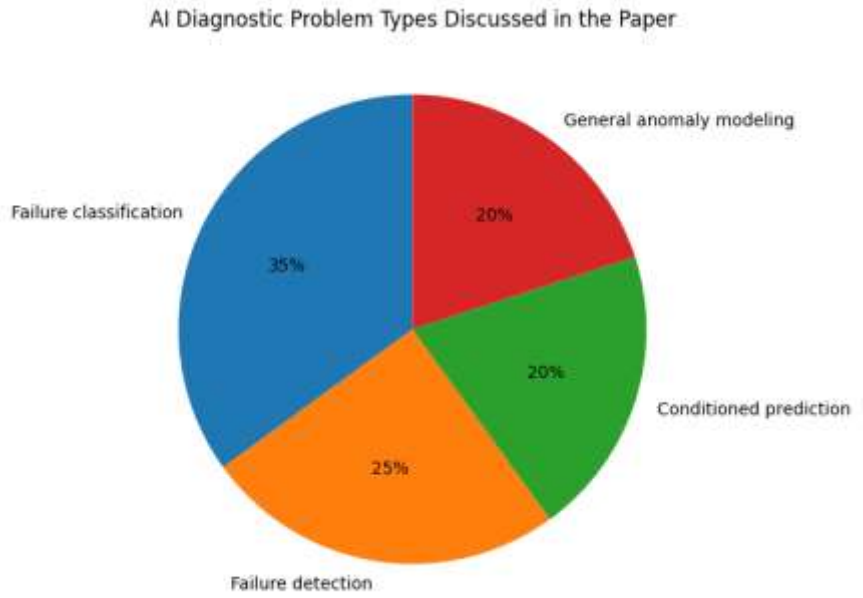
As semiconductor manufacturing is becoming increasingly complex, so are the test-based failures. Traditionally, the analysis of these failure modes was carried out manually by engineers and specialists. However, the growing number of chips to test—with the associated volume of potential test-based failures—has prompted the industry to look into solutions that improve the cadence, automation, and cost efficiency of the analysis. To address this challenge, AI has been adopted as a solution to fill the gap of human expertise. One example from the automotive industry is a Deep Learning-based failure classification model provided with redesign recommendations. Such applications necessitate the consumption of not only test-side information but also traditional design-for-test information. These relationships, however, are not always straightforward.

Four different AI problems can be identified based on the designer's goal concerning the classification and the provided input. Failures can either be classified or detected, while the model can be conditioned either with an input feature that strongly helps to predict the failure or in the most general form. There are two main reasons that explain why traditional supervised classification is not sufficient. First, a chip can be affected by too many failure modes. Second, semiconductor manufactures follow a test-based strategy, which often leads to unbalanced data—presence of a failure in a limited number of tested samples compared to its total amount. The proposed AI-powered chip diagnostics accounts for these issues and consists of a combination of multiple AI models.



5.1.DiagnosticModelsandTrainingRegimes

Reliable chip diagnostics not only help manufacturers identify the chip failure reasons but also aid design engineers to figure out possible design flaws. Unfortunately, there are no

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adequate solutions publicly available to facilitate scalable chip diagnostics modeling. Given the increasing complexity of modern chips, traditional diagnostic modeling approaches such as manually designed rules or expert systems may become impractical. Consequently, various state-of-the-art deep learning-based techniques for failing chip diagnostic modeling have been developed but generally offer poor performance. These techniques share several limitations. First, they use a multi-layer perception as a classifier, which is commonly believed to be less effective than convolutional neural networks (CNNs) when modeling classification tasks. Second, they are trained either in a single-stage or in a two-stage manner during the whole chip-level classification process. However, the two-stage training configuration introduces layer-wise category imbalance in the first-stage model, which may further introduce suboptimal first-stage models. Last but not least, these techniques lack a diagnostic failure-path analysis which helps designers to identify potential circuit design errors.

To address these limitations, researchers propose a novel diagnostic modeling framework for failing chip classification named ChipDiags, which comprises two stages: a diagnostic model and a following diagnostic sub-category analysis. A CNN-based deep learning configuration is adopted in the diagnostic modeling. The first stage investigates the chip diagnostic model training via an end-to-end level-failing-chip classification scheme, and the second stage develops a sub-category analysis system that is capable of shining a light along the failure paths of malfunctioned chips and identifying the abnormal circuit areas contributing most to the chip failure.

Table 5. AI-Powered Chip Diagnostics Models

AI Model Type	Function	Input Data	Expected Outcome
Failure Classification Model	Categorize chip failures	Test telemetry and logs	Failure categories
Failure Detection Model	Detect abnormal chip behavior	Real-time test data	Fault alerts
CNN-Based Diagnostic Model	Deep learning-based defect analysis	Chip diagnostic datasets	Improved classification accuracy
Predictive Diagnostics Model	Predict future chip failures	Historical testing patterns	Preventive maintenance
Sub-Category Analysis System	Analyze failure paths	Diagnostic outputs	Root-cause identification

6. Conclusion

The presented work illustrates a robust, scalable system architecture for the cloud-scale data engineering of semiconductor testing and diagnostics. Real-time consistency and fault tolerance requirements are met through a combination of open-source tools for data ingestion, quality control, storage, and analytics. Data is streamed in real time from semiconductor test stations during wafer manufacturing. Test vector quality is monitored and outliers highlighted for analyst review. The diagnostics subsystem deploys an advanced set of AI-powered machine learning models that reduce lab testing time in production by several orders of magnitude. These models are designed to withstand concept drift, with automatic retraining triggered by data quality monitoring.

Data engineering pipelines that serve as the foundations of semiconductor artificial intelligence are also described. New test data are ingested into the data lake on a per-test-case basis as they are generated during manufacturing. The test-condition space is monitored for gaps and the quality of surrounding test data is shown to affect AI model accuracy.

Table 6. Comparison Between Traditional and AI-Based Diagnostics

Feature	Traditional Diagnostics	AI-Powered Diagnostics
Analysis Method	Manual engineering analysis	Automated machine learning
Scalability	Limited	Highly scalable
Processing Speed	Slow	Real-time or near real-time
Failure Detection	Rule-based	Data-driven and adaptive
Handling Large Data Volumes	Difficult	Efficient
Predictive Capability	Limited	Strong predictive analytics
Cost Efficiency	High operational cost	Reduced operational cost

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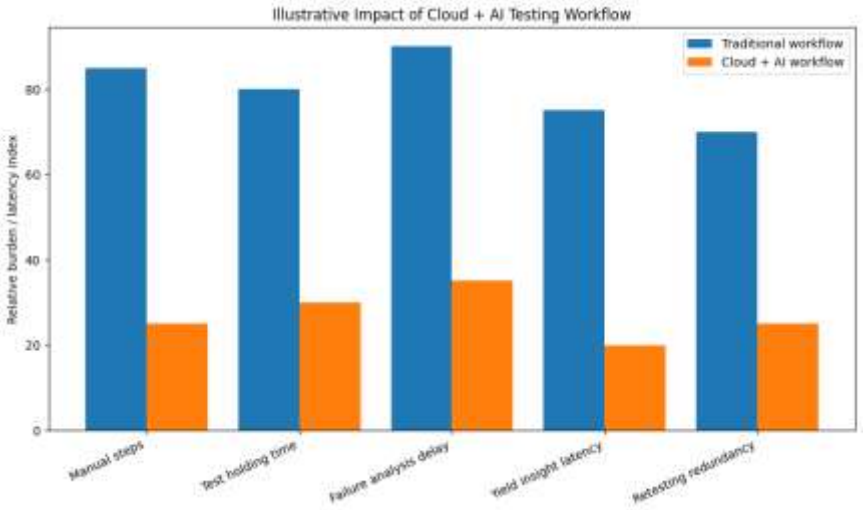

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